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METHOD OF FABRICATING CONTACT HOLES ON A SEMICONDUCTOR CHIP

Abstract

A method of fabricating contact holes on a semiconductor chip with a plurality of gates and a first mask layer includes filling a dielectric layer into the inter-gate space of two gates, polishing the dielectric layer until the surface of the dielectric layer is coplanar with the gates, depositing a second mask layer, etching the second mask layer to form a bit line opening in an array area and simultaneously forming a gate opening and a substrate opening in a periphery area, removing a portion of the dielectric layer through the bit line opening and the substrate opening to form a bit line contact hole and a substrate contact hole, filling a metal layer into the bit line contact hole and the substrate contact hole, and etching the first mask layer through the gate opening to form a gate contact hole.